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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,332	06/08/2000	Nicholas P. Cowley	P/50594/MARKS	9949

7590 08/12/2003

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EXAMINER	
PATHAK, SUDHANSHU C	
ART UNIT	PAPER NUMBER
2634	4

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,332	COWLEY ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-to-15 are pending in the application.

Drawings

2. Figures 1 & 2 should be designated by a legend such as -Prior Art-because only that which is old is illustrated. Correction is required.

3. The drawings are objected to because no arrows are used to indicate the direction of signal flow between the interconnecting elements of the system. Correction is required.

Claim Objections

4. Claim 11 is objected to because of the following informalities:

Claim 11 refers to a "programmable divider", but is later referred to as only a "divider". Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, 13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Nolde et al. (4,607,393).

Regarding to Claim 1, Nolde discloses a receiver circuit comprising an oscillator arrangement and a multiplier (Figure 1). The multiplier (Fig. 1, element 2) having a first input for receiving an input signal (Fig. 1, element 1) and the second input

connected to the said oscillator arrangement. The reference describes the oscillator arrangement comprising of a first oscillator (Fig. 1, element 7) for supplying the second input to the said multiplier, a second oscillator (Fig. 1, element 11) for producing a second signal in a separate frequency band, and a reference pilot signal (Fig. 1, element 18). Nolde also discloses the oscillator arrangement to consist of two phase locked loops, wherein the first oscillator is phase locked to said second oscillator and said second oscillator being phase locked to the said reference pilot signal (Abstract, lines 2-11).

Regarding to Claim 2, Nolde describes the output of the output signal of the second oscillator to be 4.56MHz (Preferred Embodiments, paragraph 3, line 4), and the output of the first oscillator, also the second input to the multiplier, to be such that the difference between the input VHF (30-300MHz) signal and the output of the first oscillator to be 10.7MHz. Therefore, the second frequency band is lower than the said first frequency band.

Regarding to Claim 13, Nolde discloses a second oscillator (Fig. 1, element 11) and the said reference signal forming a phase locked loop comprising a second divider (Fig. 1, element 13), a third divider (Fig.1, element 14), and a second comparator (Fig. 1, element 15). These elements are connected wherein the first input is connected via the second divider to the second oscillator and the second input connected via the third divider to the reference signal.

Regarding to Claim 15, Nolde discloses a frequency tuner circuit comprising an oscillator arrangement and a multiplier (Figure 1). The multiplier (Fig. 1, element 2)

having a first input for receiving an input signal (Fig. 1, element 1) and the second input connected to the said oscillator arrangement. The reference describes the oscillator arrangement comprising of a first oscillator (Fig. 1, element 7) for supplying the second input to the said multiplier, a second oscillator (Fig. 1, element 11) for producing a second signal in a separate frequency band, and a reference pilot signal (Fig. 1, element 18). Nolde also discloses the oscillator arrangement to consist of two phase locked loops, wherein the first oscillator is phase locked to said second oscillator and said second oscillator being phase locked to the said reference pilot signal (Abstract, lines 2-11).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolde et al. (4,607,393) in view of Kunkel (6,370,360).

Regarding to Claims 3-5, Nolde discloses all the subject matter claimed except the frequencies specified. Nolde describes his invention to operate in the VHF band (30-to-300MHz), for FM receiver applications. However, Nolde does not specify that this invention could be implemented at different frequency bands.

Kunkel discloses a communications unit comprising a receiver in one or more frequency ranges with associated channel spacing (Abstract, lines 1-4). Kunkel discloses a frequency synthesizer comprising an oscillator arrangement wherein the first oscillator is phase-locked to a reference oscillator (Column 2, paragraph 2, lines 15-20). The oscillator signals are used in receivers to select a certain channel in a frequency band when mixing with an incoming input signal (column 1, paragraph 4, lines 44-55). The intention of the frequency synthesizer is to generate oscillator signals for multiple applications at different frequency ranges with large (mobile telephony) and small (satellite) channel spacing (Column 2, paragraph 3, lines 33-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the UHF band or 950-2150MHz, or 400-600MHz, because this is a matter of design choice and there is no criticality in the particular frequencies.

9. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolde et al. (4,607,393) in view of Behrent (5,896,061).

Regarding to Claims 6, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. However, Nolde does not specify a low pass filter wherein the said first multiplier having an output for supplying an input signal to said low pass filter.

Behrent discloses a receiver circuit (Fig. 1), wherein the output of multiplier (Fig. 1, element 4) is connected to the input of the low pass filter (Fig. 1, element 6).

The lowpass filter provided for the suppression of undesired mixing products and carrier residue (column 3, lines 27-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by implementing a low pass filter at the output of the multiplier would increase the sensitivity of the receiver.

Regarding to Claims 7, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. However, Nolde does not specify a low pass filter connected to the output of the first multiplier.

Behrent further discloses that the filter should be selected such that the frequency deviation (the difference between the local oscillator frequency and the input signal carrier frequency) must lie within the transmission range of the filter (column 4, paragraph 4, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a cut-off frequency band of the low pass filter in the range of 5-40MHz because this is a matter of design choice and there is no criticality of these particular frequencies.

Regarding to Claims 8, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. However, Nolde does not specify a second multiplier having a first input for receiving the said input signal and a second input connected to said oscillator arrangement for receiving a quadrature signal.

In Figure 1, Behrent further discloses a second multiplier (Fig.1, element 15) having first input for receiving said input signal and a second input connected to an oscillator for receiving a quadrature signal. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to implement an in-phase (I) and quadrature (Q) topology for PSK, QAM, etc. modulation schemes to increase the throughput of the receiver.

Regarding to Claims 9, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. However, Nolde does not specify a phase adjusting network to which the first oscillator is connected, for forming said first signal and said quadrature signal.

Behrent discloses an oscillator (Fig. 1, element 11) that is connected to a phase adjusting network (Fig.1, element 13) supplying the said first signal (Fig.1, element 12) and the quadrature signals (Fig.1, element 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by adding the phase adjusting network as described in Behrent to the first oscillator as described in Nolde, provides an enhanced receiver capable of receiving both in-phase and quadrature signals, and increasing the receiver throughput.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nolde et al. (4,607,393) in view of Behrent (5,896,061) in further view of Gopinathan et al. (6,188,291).

Regarding to Claim 10, Nolde in view of Behrent discloses a receiver circuit comprising of a two multipliers, a low pass filter, a quadrature phase shifter and an oscillator arrangement as described above. These references do not disclose the circuit topology used for the first oscillator and the phase shifter.

Gopinathan discloses (Fig. 1B) a ring oscillator configuration so as to generate a plurality of signals but shifted in phase. The oscillator signals can be used to provide quadrature signals for driving mixers where accuracy of the quadrature phase relationship is necessary (column 1, Background of Invention, lines 10-20). Such an oscillator arrangement provides a quadrature phase difference accuracy in the order of 0.05 degrees over a 40MHz tuning range at a center frequency of 900MHz (Column 4, lines 24-27). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the invention as described in Gopinathan can be used as the first oscillator in the said oscillator arrangement for supplying the first and said quadrature signals, to provide a frequency and phase stable output signal generated by the oscillator.

11. Claim 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolde et al. (4,607,393) in view of Gardner (Phaselock Techniques, 2nd Edition, Copyright 1979).

Regarding to Claim 11, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. The reference does not specifically show the same configuration of the oscillator arrangement.

However, Gardner in Figure 10.9 (Chapter 10, Frequency Synthesizers, Page 209) discloses a basic phase locked synthesizer consisting of a first oscillator (Fig. 10.9, element "fo") and a reference oscillator (Fig. 10.9, "fr") wherein the first oscillator is phase-locked to the second oscillator. Gardner further describes the phase lock loop to comprise of a first programmable divider, a first comparator

having an output, a first input connected via said first divider to said first oscillator and second input connect to second oscillator, and a first control loop connected between said output of said first comparator and said input of said first oscillator. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the teachings of Gardner to implement a first divider better facilitates the synchronization and locking of the desired frequencies of the oscillator arrangement.

Regarding to Claim 12, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. The reference does not explicitly specify the first programmable divider to have selectable values of two, three and four.

Gardner discloses dividers to be integers selected to provide a certain output frequency, digital counters are used almost exclusively in this service (Chapter 10, Frequency Synthesizers, Page 209, Paragraph 2, lines 1-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the teachings of Gardner to implement a first divider to use any integer value for the divider to obtain the desired frequencies of the oscillator arrangement.

12. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nolde et al. (4,607,393) in view of Mittel et al. (5,789,987).

Regarding to Claim 14, Nolde discloses a receiver circuit comprising of a multiplier and an oscillator arrangement as described above. However Nolde does not disclose weather the receiver a monolithic IC.

Mittel discloses a communications receiver comprising a receiver element. The receiver element includes a reference oscillator, and frequency synthesizer. The frequency synthesizer comprises a main PLL and a tracker PLL, a loop filter, frequency dividers (Fig.1, element 100). All circuits are integrated in the same monolithic device (Abstract, lines 3-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Mittel teaches us that the receiver circuit components as described in Nolde can be integrated in the same monolithic device, to reduce complexity, minimize alignment of external components minimize cost and to save space.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703) 305-0341. The examiner can normally be reached (Monday-Friday from 8:30 AM to 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 20231

Or faxed to: -

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Part II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

July 24, 2003
Sudhanshu C. Pathak -- Examiner Art Unit 2634

STEPHEN CHIN
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